

SOC H.264 AVC Video Decoder IP Core Datasheet

System-On-Chip (SOC) Technologies

1. Key Features

1. Profile&Level: High profile (up to 4.2L)
2. Chroma Format: 4:2:0 or 4:2:2
3. Frame Rate: up to 120fps
4. Resolution: SD (STSC and Pal), 720i, 720p, 1080i, and 1080p
5. Precision: 8 or 10 bits
6. Input Stream: Transport or Elementary
7. Latency: 0.25ms
8. Minimum FPGA: Xilinx Spartan-6 LX75
9. Multiple streams: Example: 4 Streams on Xilinx Kintex-7 K410

2. Product Overview

The SOC H.264 AVC video decoder IP Core is a single chip solution that supports single or multi-stream H.264 video decoding for all industrial standard resolutions including QVGA, SD and HD up to 1080p/120fps. The SOC H.264 4k and 8k decoders are released as separated products.

SOC provides the versions of the H.264 video decoder IP core for FPGAs of Xilinx, Altera, and Microsemi. SOC also supplies all-in-one decoder modules based on the same H.264 video decoder IP core. Refer to the Product Brief and Datasheet for SOC MPEG codec modules for details.

The SOC H.264 AVC video decoder is implemented based on SOC's proprietary single-clock driven all-hardware technology (without microprocessors or embedded software), which has significant advantages of high-speed (low latency), small footprint (low power), high video

quality, and high resolution. The decoder fits into a small footprint FPGA, for example, the low end Xilinx Spartan-6 series, such as the XC6SLX100.

The SOC H.264 AVC video decoder is at high-profile and backward compatible with main and simple profiles according to the MPEG standard. It decodes both 4:2:0 and 4:2:2 streams with automatic selection. The decoder is suited for both consumer products and high-end applications such as broadcast, digital cinema, military, and medical devices. It is also well suited for smart cell phones and mobile devices, as it has low power consumption.

The SOC decoder series can be integrated with an audio decoder to provide an all-in-one decoding solution. SOC also integrates network modules, TCP/UDP-IP, Ethernet MACs, as well as the MPEG transport de-multiplexer into the design to produce full system-on-chip systems. Customized versions of these products are available on request.

Refer to the [Integration Sheet](#) for details of integrating the H.264 Encoder IP Core into a user system.

3. The SOC H.264 AVC Video Decoder Architecture

Fig. 1 is the block diagram of the SOC H.264 AVC video decoder. It is a self-contained FPGA IP core that can be either placed into a single FPGA or integrated with other logic blocks in the same FPGA for system-on-chip solutions.

All of the blocks in the design, shown in Fig. 1, are implemented in hardware without embedded processors or embedded software, which offers high speed, low logic resource consumption, and low power. Input to the decoder is standard H.264 elementary stream without bit rate limitation. The output of the decoder is the video stream for standard display devices with frames properly ordered. SOC also provides an MPEG transport decoder to allow the input to the decoder to be in the form of MPEG transport streams.

The decoder also automatically detects missing data, if any, and compensates for the missing blocks using the corresponding blocks in the neighboring frames to increase the overall video quality.

The SOC H.264 video decoder requires two external clock sources with one at 100MHz and the second at 27MHz. The decoder also requires an external DDR3 memory of minimum of 256MB for 1080p resolution (for both 30fps, 60fps, and 120fps).

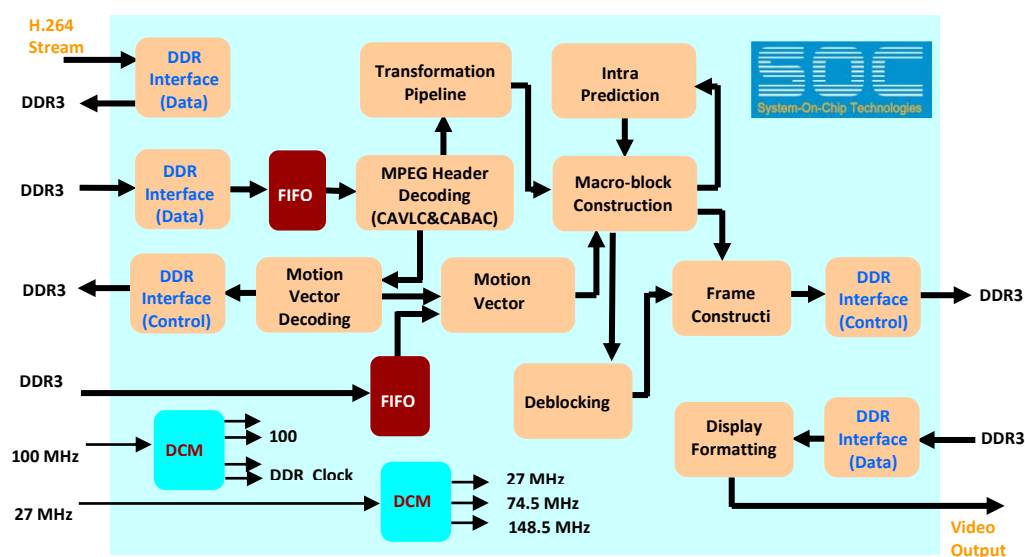


Fig. 1 Block Diagram of SOC H.264 AVC video decoder

4. Technical Specifications

Conformance Standard:

H.264/AVC (ISO/IEC14496-10)

Profile:

The SOC H.264 decoder supports:

- Simple Profile
- Main Profile, and
- High Profile.

Level:

The SOC H.264 video decoder supports all the levels, which include:

- Low Level
- Main Level
- High-1440 Level, and
- High Level.

Chroma Forma:

The SOC H.264 video decoder supports:

- 4:2:0
- 4:2:2
- 4:4:4 (on request)

Precision:

The SOC H.264 video decoder supports:

- 8 bits
- 10 bits.

Inter Frames:

The SOC H.264 video decoder supports:

- I frame
- P frame
- B frame.

Frames Rates:

The SOC H.264 video decoder supports all standard frame rates:

- 10fps, 24fps, 25fps, 29.97fps, 30fps
- 50fps, 59.95fps, 60fps
- 120fps (on request).

Resolutions:

The SOC H.264 video decoder supports all standard resolutions (both NTSC and Pal):

- SD, 720i, 720p, 1080i, 1080p

Input Data Rate:

There is no limitation on the data rate of the input streams, as long as it is H.264 compliant.

Latency:

The SOC H.264 video decoder has very low latency due to its hardware implementation. The decoding engine latency is less 0.25ms from data in to data out. The decoder can buffer 1 complete frame before display, if needed, to compensate any jitters of the input stream, which is controllable through the API.

Power:

The power consumption is less than 800mw for the core only. If the core is mapped for ASIC production, the power consumption will be considerably less.

A summary of these specifications is provided in Table-1.

Table-1 Specification Summary Table

FEATURE	DESCRIPTION
MPEG Profile	High
MPEG Level	Up to High-1440
Resolution	QVGA, SD, and HD up to 1080p @30 or 60fps (2k and 4k resolution available under a separate product release)
Input bit rate	There is no input bit rate limitation

Latency	0.25 ms
Power	< 800mw (on Xilinx Spartan-6 FPGAs)
Interlace Stream	Support
FPGA size	Spartan-6 LX75 single channel for 1080p/60fps
Multiple channels	2 channels on Spartan-6 LX150, 4 channels on Kintex-7 K325
Integrated Audio decoder	Available
MPEG Transport DeMux	Available
Ethernet MAC	Available for integration
UDP/TCP-IP	Available for integration
User defined I/O	Supported
Copy to ASIC	Supported

5. Targeted FPGAs and Logic Resources

The SOC-H.264-S6 fits into a low-end Spartan-6 FPGA, such as the LX75 for HD 1080p/60fps.

The SOC H.264 video decoder fits most of the Xilinx FPGAs, such as:

- Spartan-6
- Virtex-6
- Kintex-7
- Virtex-7
- Artix-7

Decoder IP cores are also available for Altera FPGAs, including:

- Cyclone-V
- Arria-V
- Stratix-V

Logic Resources on Xilinx FPGAs:

The logic resources required on Xilinx FPGAs by the H.264 decoder IP core is listed in Table-1

Resources type	Resource Utilization
LUTs	60k
B-RAM	5Mbits
DSPs	25

Table-1 Logic resource utilization of the H.264 decoder for up to 60fps

Logic Resources on Altera FPGAs:

The logic resources required on Altera FPGAs by the H.264 encoder IP core is listed in Table-2

Resources type	Resource Utilization
ALM	40k
B-RAM	5Mbits
DSPs	25

Table-2 Logic resource utilization of the H.264 decoder for up to 60fps

FPGA Examples:

The following Table-3 shows the FPGA examples for 1080p@30, 1080p@60, and 1080p@120 resolutions. Other FPGAs are also supported, as long as the logic resources and clock speed meet the requirement.

Resolution@frame-rate	Xilinx FPGA Example	Altera FPGA Example
1080p@30	Spartan-6 LX100	Cyclone-5 5CGTD9
1080p@60	Artix-7 XC7A100T	Arria-10 GX160
1080p@120	Artix-7 XC7A200T	Arria-10 GX220

Table-3 Examples for Xilinx and Altera FPGAs

6. Applications

- TV set-top Boxes
- IPTVs
- Video conferencing devices
- Consumer products
- Smart cell phones

- Satellite video/audio transmission equipment
- Digital cinemas
- Broadcast Equipment
- Medical imaging devices
- Military applications
- Others

The SOC H.264 video decoder is designed for high-performance, but it can also be used for low-end application, such as video surveillance products. SOC provides customizations for these products.

7. Using the SOC H.264 Video Decoder

SOC provides three packaging formats to customers, which allows for easy-of-use of the product. These formats include:

1. FPGA IP core
 - A self-contained IP core for FPGA users, in either bit file or encrypted netlist. An integration datasheet is provided, when the netlist is delivered.
2. SOC MPEG Codec Modules
 - SOC provides all its codecs, including the H.264 decoder, on a small circuit board that integrates all required components for video or audio or both video and audio encoding/decoding. The codec module connects to a host device via a PCB connector. SOC also provides evaluation/development kits for the modules and IP core.
3. Customized system-on-chip solutions surrounding the decoder
 - SOC provides integration with other IP cores to produce a system-on-chip solution.

Technical data for using the above three formats are described in the following sub-sections.

8. The H.264 Video Decoder IP Core Integration Sheet

When the decoder is delivered in IP core format, it is a ready-to-use bit-stream core for FPGAs. SOC supports both Xilinx and Altera FPGAs according to user requirement. Fig. 2 shows the inputs and outputs of the decoder core.

The H.264 video decoder IP core integration details are provided in a separate document under the title of “H.264 Video Decoder IP Core Integration Sheet”.

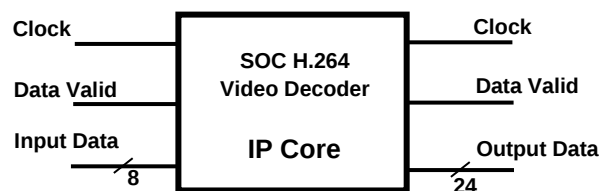


Fig. 2 The inputs and outputs of the H.264 IP Core

9. The H.264 Video Decoder Modules

SOC supplies the MPEG4-AVC/H.264 decoder on a 2.7”x1.7” or 2.7”x2.0 module (card), as shown in Fig. 3. The modules provide complete function of video/audio decoding. The module connects to the host product/PCB via a device-to-PCB connector, as shown in Fig. 4.



Fig. 3. SOC H.264 Decoder Module



Fig. 4. Device-to-PCB connectors

The SOC MPEG Codec Modules can be directly connected to I/O interface chips for product fabrication, as shown in Fig. 5, or connected to an FPGA or a Microcontroller for user system integrations, as shown in Fig. 6.

Refer to the Product Brief and Datasheet of SOC MPEG Codec Modules for technical details.

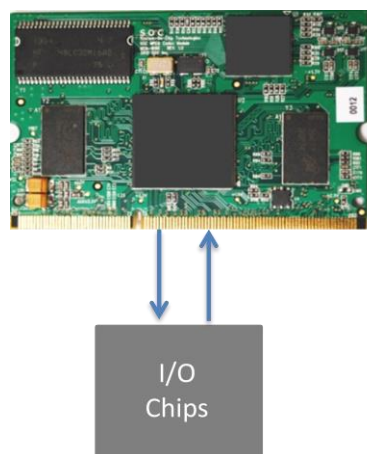


Fig. 5 SOC MPEG Codec Module directly connects to I/O interfaces in user product

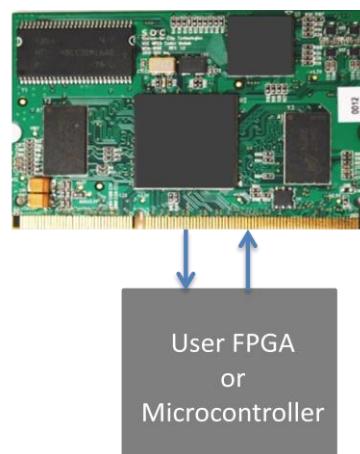


Fig. 6 SOC MPEG Codec Module connects to FPGA/microcontroller for user integration

10. The H.264 HD Decoder Chipset

SOC-M_{Codec}™

SOC Technologies provides a series of CODEC chipsets, the SOC-Mcodec family, which can be dropped onto user PCBs as ASIC video encoders and decoders. The SOC-Mcodec family of chipsets support all MPEG standards, including H.264, H.265, and MPEG-2, and all industrial standard resolutions, including SD, 720, 1080, 4K, and 8K, with frame rates of up to 120 fps.

The SOC H.264 HD Decoder Chipset includes an FPGA and FLASH preconfigured with SOC's H.264 HD Encoder IP Core. It is an ASIC that receives raw video/audio and outputs an H.264 video stream with optional AAC/MP2/MP3 audio compression. It supports resolutions up to HD at 60 fps.



Fig. 5 SOC-Mcodec chipsets

SOC CODEC Chipsets are fully pre-configured FPGA chips that are designed to function just like traditional ASIC chipsets, integrated onto user PCB by connecting the pins.

The Chipset I/O interfaces can be customized to virtually any customer specifications, making them the most flexible CODEC chipsets on the market. This is especially useful if your system demands non-standard I/O interfaces - let us tailor the interfaces to work in harmony with your system.

Unlike traditional ASICs, SOC's CODEC chipset firmware may be updated to change its functionality or I/O interfaces if needed.

The SOC CODEC Chipsets are built using SOC Technologies' portfolio of ultra-high-performance CODEC and peripheral IP Cores. You can expect high quality, high speed, low latency, and low power-consumption.

With high volume productions of FPGAs, today's FPGAs are fabricated using the most current silicon technologies that are used for computer CPUs, such as the new 10nm silicon class. This makes the FPGA based ASICs away ahead of the traditional MPEG codec ASICs, especially in power consumption, speed, and cost.

11. Customized System-on-Chip Solutions Surrounding the Decoder

SOC also provides customized system-on-chip integrations based on the H.264 video/audio decoders. Fig. 7 shows an example of an integrated decoder solution for HD video over the Internet with HDMI output.

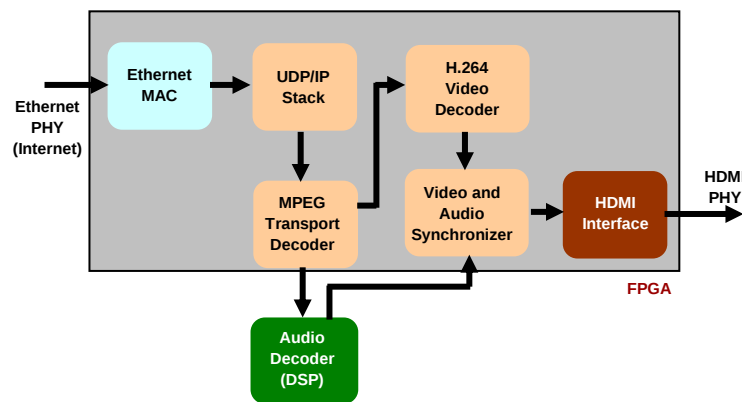


Fig.7 Example system-on-chip solution: HD-over-IP decoder

12. MPEG-2 and H.264 Multi-protocol Decoder

SOC also offers a combined (multi-protocol) MPEG-2 and H.264 video decoder, as shown in Fig. 8, to allow the decoder to decode either MPEG-2 or H.264 automatically according to the input stream. All the product formats discussed in Section 7 are available for the multi-protocol decoder. This multi-protocol MPEG video decoder can also be configured to decode both MPEG-2 and H.264 streams con-currently.

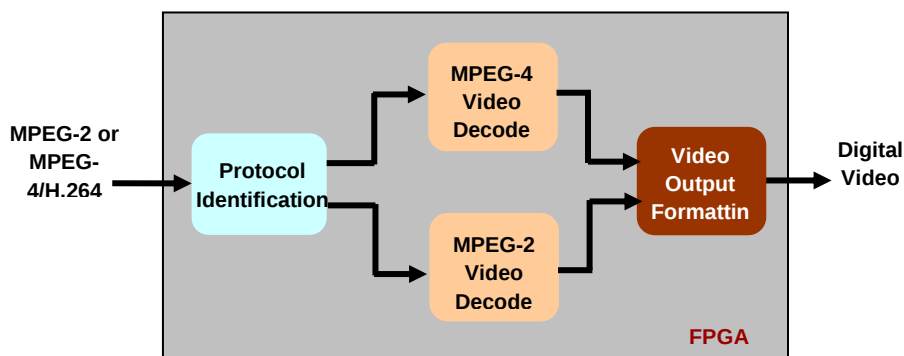


Fig. 8 Multi-protocol video decoder

Fig. 9 shows the block diagram of the multi-protocol video/audio decoder. One FPGA and one DSP are used in the system to achieve high-performance and low cost. Similar to the video only decoder shown in Fig. 8, the video/audio decoder can also be configured to decode two MPEG transport streams with one being the MPEG-2 and the other being the H.264.

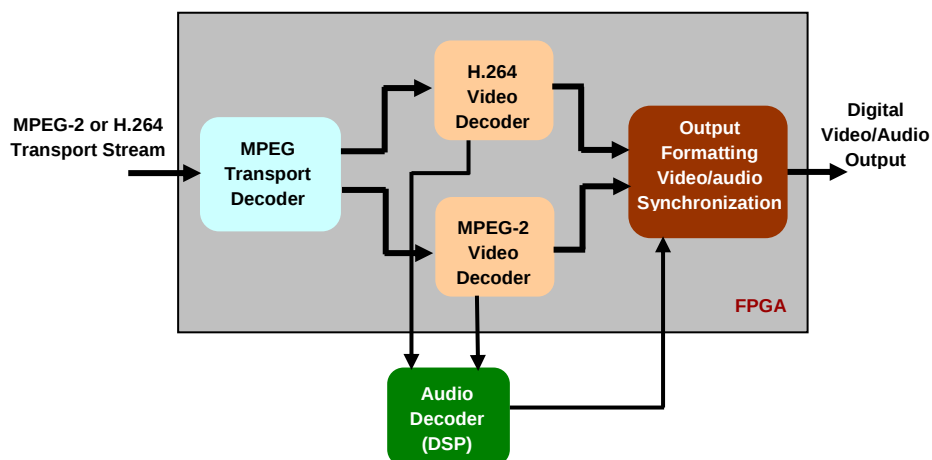


Fig. 9 Multi-protocol video/audio decoder

13. The SOC Product Code Format

SOC integrates its products of MPEG Codecs into one Product Code system, as shown in Fig. 10. The following products use the same Product Code system.

1. H.264, H.265, and MPEG-2 encoder and decoder IP cores (HD, 4K and 8K)
2. H.264, H.265, and MPEG-2 encoder and decoder Modules (HD, 4K and 8K)
3. Codec IP core or module evaluation kits
4. OEM products.

SOC Product Code Format

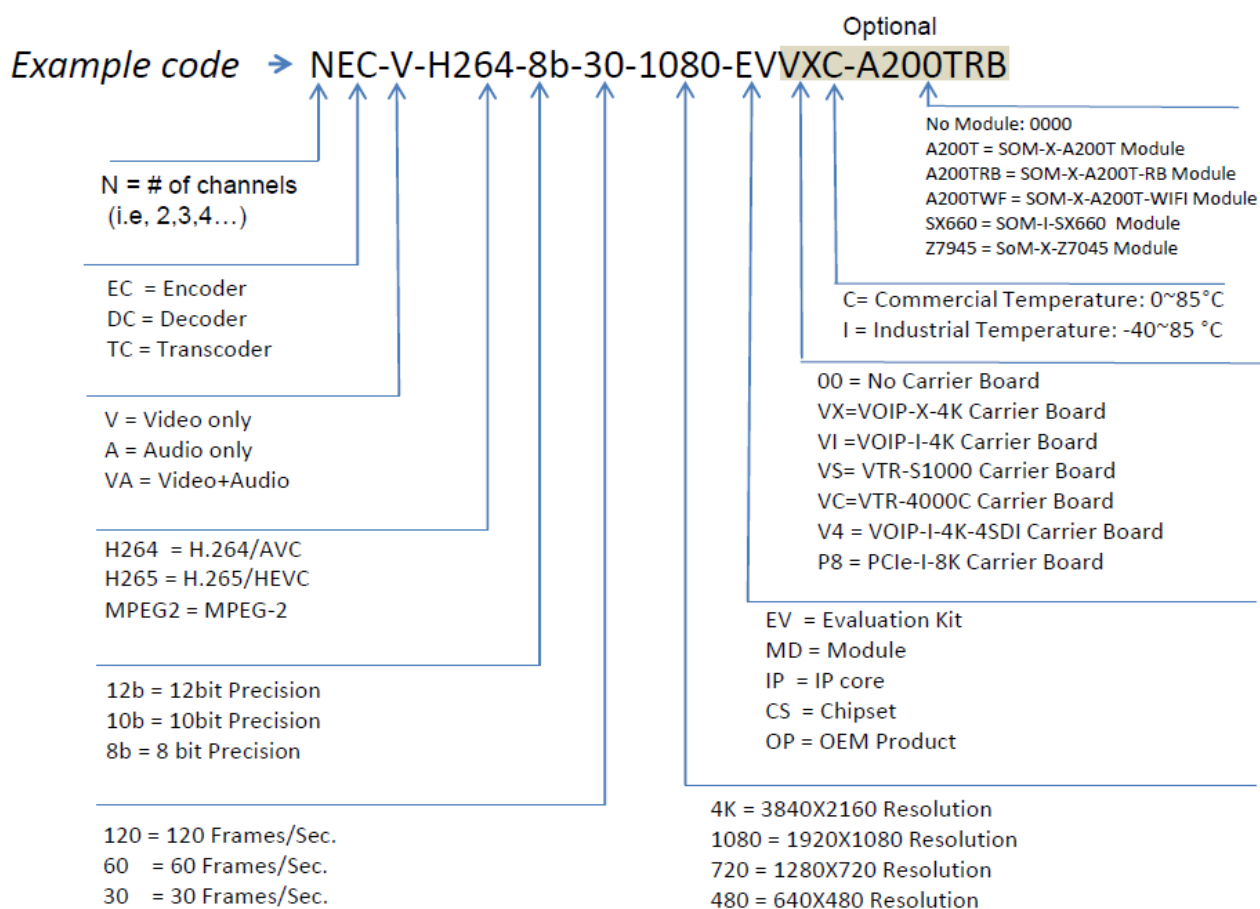


Fig. 10 The Product code system for the SOC codec products

14. Technical Support

SOC provides technical support for all its products, which include documentation, web site based, and telephone based support. Additional support services, such as on-site training services, can be subscribed from SOC as a service contract.

15. IP core upgrading

Upgrades to the IP core are available to all the delivery formats discussed in Sections 7 and 8. Upgrade is usually a part of the technical support contract signed individually. On-line automatic upgrading can also be arranged if desirable.

16. Related Information

The SOC MPEG-2 video decoder is implemented based on the same technology of this H.264 decoder. The only difference between the MPEG-2 and the H.264 decoders is the MPEG standard, while the MPEG-2 decoder is MPEG-2 compliant, the H.264 decoder is MPEG-4 part-10 AVC compliant. The datasheet of SOC MPEG-2 video decoder resembles this datasheet in many ways, as the two decoders are similar in terms of architecture and functionality, except for the standards.

17. Related Documents

1. Integration Sheet – Decoder IP Cores
2. API Manual – H.264 Decoder IP Core
3. Pin Assignment Sheet – Decoder Modules
4. Pin Assignment Sheet – Decoder Chipsets

18. Ordering Information

The SOC H.264 video/audio decoder IP cores are available for licensing or a combination of one-time fee plus reduced royalty payments.

The SOC H.264 video/audio decoder module is a complete solution for video and audio decoding at low cost. It is sold on a unit by unit basis without limitation on the quantities.

SOC also provides integration of the H.264 decoder with other functional IP cores of SOC or customer provided IP cores. A combination of NRE and licensing royalties is normally considered, which is negotiated on a case by case basis.

Please contact SOC sales by telephone +1 519 880-8609 or e-mail: sales@soctechnologies.com

19. Document Revisions

Version #	Revision Date	Notes
V.1.0	2009/11/15	First release
V.1.1	2010/05/10	
V.2.0	2011/08/15	Major revision
V.2.1	2012/05/15	
V.3.0	2012/11/15	Major revision
V.3.1	2013/08/10	
V.4.0	2014/03/15	Major revision
V.4.1	2015/11/10	
V.5.0	2016/05/18	Major revision
V.6.0	2020/03/12	Major revision